Power source apparatus for driving liquid crystal display.

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Abstract

A plurality of resistors (11 - 17) serially connected with each other between a maximum voltage level "V" and a minimum voltage level "0" are provided to generate voltage-divided intermediate voltage levels "V2H", "V1H", "V3L", "V2L", the voltages having the voltage-divided intermediate voltage levels being supplied to a first group of operational amplifiers (19, 20) whose first stage input portions are formed of N-channel MOSFETs and a second group of operational amplifiers (21, 22) whose first stage input portions are formed of P-channel MOSFETs. Frame signal FR for alternating-current-driving a liquid crystal display device is supplied to the operational amplifiers. When signal FR is in a state "0", the first group of operational amplifiers are brought into an active state while the second group is brought into an inactive state. When signal FR is in a state "1", the first group of operational amplifiers are inactive. Under the condition that power down signal PD for non-use of the liquid crystal display device is generated, all of the operational amplifiers are controlled to be in an inactive state.

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(54) Power source apparatus for driving liquid crystal display.

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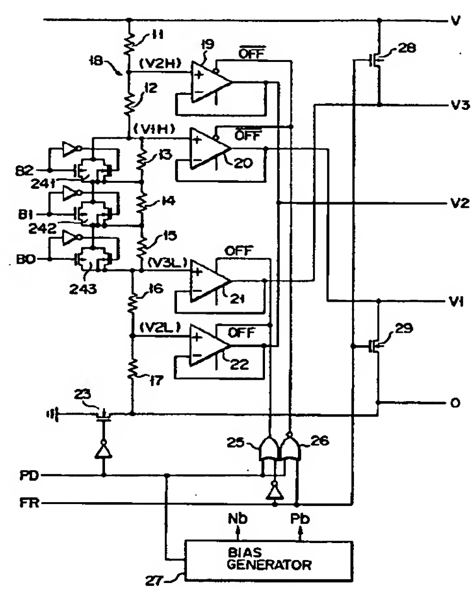


F I G. 1

EP 0 479 304 A2

The present invention relates to a liquid crystal display device driven by an alternating current, especially to a power source apparatus which is used for driving a liquid crystal display device and has four intermediate potentials between a maximum potential and a minimum potential.

A liquid crystal display device has an arrangement of a plurality of display dots, which are formed of cross points of a group of segment electrodes and a group of common electrodes. The liquid crystals between the two groups of electrodes are controlled in their crystal arrangement by means of potential difference between the groups of segment electrodes and the group of common electrodes in order to display images.

Such a liquid crystal display device uses a dynamic driving control in which potentials set between the segment electrodes and the common electrodes are generally reversed in polarity for each frame. For such a dynamic driving control, there are generally prepared power sources for providing four intermediate potential levels in addition to a maximum potential power source and a minimum potential power source, the intermediate potential levels being obtained by dividing the potential difference between the maximum potential level and the minimum potential level into four parts. A power source having a suitable potential level is selected in accordance with a display data, and the voltage obtained by the selected potential power source is delivered and applied to the group of segment electrodes and the group of common electrodes.

The four intermediate potential levels between the potential levels set by the maximum potential power source and the minimum potential power source are generated by a voltage dividing circuit which is formed by a combination of resistors.

Fig.8 shows a conventionally known power source circuit for driving a liquid crystal display device. This power source circuit is arranged such that any one of terminals V1, V2, and V3 supplies, corresponding to frame signal FR, a power source output having a predetermined potential for A.C.-driving a liquid crystal display device.

For instance, as apparent from the relationship shown in Fig.9 and the timing chart shown in Fig.12, the maximum potential level "V", the two intermediate levels "V2H" and "V1H", and the minimum potential level "0" are put out when frame signal FR is "0", whereas, when frame signal FR is "1", the maximum potential level "V", the two intermediate potential levels "V3L" and "V2L", and the minimum potential level "0" are put out. These potential level combinations are alternately generated whenever the frame signal changes between "0" and "1". These potential signals are supplied through the segment output level selecting circuit shown in Fig.10 and the common output level selecting circuit shown in Fig. 11 to the segment electrodes and the common electrodes of the liquid crystal display device.

Fig.8 shows a 1/5 pre-biased power source circuit, in which resistors R1 and R4 are each set to 300 KΩ, resistors R2 and R3 to 100 KΩ, resistors r1 and r4 to 30 KΩ, and resistors r2 and r3 to 10 KΩ. The dynamic chart shown in Fig. 12 shows a case of a 1/8 duty in which the number of common outputs is eight. The figure exemplary shows only one segment output among a plurality of segment outputs and only one common output among a plurality of common outputs.

In such a power source circuit, clock signal ϕc formed of a pulse signal indicating a common selection signal switching timing, and lowers the output resistance of the potential dividing circuit at a moment of a common signal switching time so as to increase the response of the liquid crystals. Namely, the charging or discharging time of a capacitance provided in the liquid crystal display device is made short by connecting resistors r1 - r4, which are lower in resistance value than resistors R1 - R4, in parallel with resistors R1 - R4 for dividing voltage V.

However, a large capacitance is required for a liquid crystal display device having a large number of display pixels. Therefore, the output resistance of the voltage dividing circuit must be made sufficiently small, or a satisfactory display quality may not be obtained. However, if the output resistance of the voltage dividing circuit is made small, the problem of increase in power consumption will occur.

Fig. 13 shows a circuit for making small the output resistance of the intermediate potential level power sources. In this circuit, operational amplifiers OP1 through OP4 are used to put out the voltages which are voltage-divided by resistors R1 - R5. This circuit shows a 1/5 pre-biased case, and resistors R1 - R5 are made of resistance element having a same resistance value. However, in such a circuit which uses operational amplifiers, operational amplifiers OP1 - OP4 are always set in active condition, so that the power consumption at the operational amplifier portion is large.

The object of the present invention is to provide a power source apparatus for driving a liquid crystal display device, in which the output resistance of its voltage dividing circuit can be set sufficiently small, and an image display having a good display quality may be realized.

Another object of the present invention is to provide a power source apparatus in which the output resistance may be set sufficiently small, and the power consumption at the voltage dividing circuit portion will surely be reduced.

In a power source apparatus for driving a liquid crystal display device in the present invention, the power source voltages with a plurality of voltage difference levels set by a voltage dividing circuit formed by a resistor circuit are put out through the operational amplifiers, the operational amplifiers being selectively rendered to be in an inactive state in accordance with frame signals.

The plural operational amplifiers, which are arranged for providing the plural intermediate potential levels and form the driving power source device, are selectively rendered to be in an inactive state in a period of time when a potential having a potential level corresponding to any one of the operational amplifiers is not used as a liquid crystal driving power source, so that the electric current for operating the operational amplifier reduces. In addition, the presence of the operational amplifiers assures the reduction in output resistance, and the liquid crystal display device will be kept good in quality.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a circuit diagram of one embodiment of the present invention for explaining a power source apparatus for driving a liquid crystal display device.

Fig. 2 and Fig. 3 are circuit diagrams for showing concrete examples of an operational amplifier which is a constituent of the above power source device.

Fig. 4 is a circuit diagram for showing concrete example of a bias voltage generator which is a constituent of the above power source device.

Fig. 5 is a diagram of signal waveforms for explaining the operation condition of the above power source device.

Fig. 6 and Fig. 7 are circuit diagrams respectively showing another examples of the operational amplifiers shown in Fig. 2 and Fig. 3.

Fig. 8 is a circuit diagram for showing an example of the conventional power source circuit.

Fig. 9 is a table for explaining a voltage level generating condition of the circuit shown in Fig.8.

Fig. 10 and Fig.11 respectively show circuit examples of a liquid crystal driving portion into which driving power source voltage is supplied.

Fig. 12 is a timing chart for explaining the condition of the liquid crystal driving power source voltage.

Fig. 13 is a circuit diagram for showing another example of the conventional power source circuit.

The embodiment shown in Fig. 1 is a power source circuit which is formed of a C-MOS integrated circuit and is applied to a driving device which is incorporated in a one-chip micro computer to drive a liquid crystal display device of the computer. Voltages having different intermediate levels generated by the power source circuit are respectively put out from points V3, V2 and V1. The voltages put out of points V1 and V3 are supplied to a segment output level selecting circuit shown in Fig. 10, whereas the voltage put out of point V2 is supplied to a common output level selecting circuit shown in Fig. 11.

Between a highest potential power source line to which a highest potential V is set and a lowest potential power source line to which a lowest potential 0 is set is connected a voltage dividing circuit 18 which is formed by serially connecting resistors 11 and 12, resistors 13 - 15, and resistors 16 and 17. A voltage having a voltage level "V2H" is put out of a connecting point between resistors 11 and 12, a voltage having a voltage level "V1H" is put out of a connecting point between resistors 12 and 13, a voltage having a voltage level "V3L" is put out of a connecting point between resistors 15 and 16, and a voltage having a voltage level "V2L" is put out of a connecting point between resistors 16 and 17. These voltage outputs are respectively supplied to operational amplifiers 19 to 22. Outputs from operational amplifiers 19 and 22 are put out as voltage V2, an output from operational amplifier 20 is put out as voltage V1, and an output from operational amplifier 21 is put out as voltage V3. The lowest potential power source line is grounded through N-channel MOS transistor 23.

Resistors 13 to 15 are treated as one group. They respectively have parallel connected analogue switching circuits 241 to 243 which are ON-OFF controlled by signals B0 to B2. A composite resistance value of resistors 13 to 15 is set by signals B0 to B2. Signals B0 to B2 are each an output of a processor portion, not shown in any of the drawings, and pre-bias values to be supplied to liquid crystals may be set by a program.

Operational amplifiers 19 and 20 are constructed such that an N-channel MOSFET is used at their respective first stage input portion. Operational amplifiers 21 and 22 are constructed such that a P-channel MOSFET is used at their respective first stage input portion. Fig.2 shows a circuit of an exemplary embodiment for each of operational amplifiers 19 and 20. Fig. 3 shows a circuit of an exemplary embodiment for each of operational amplifiers 21 and 22.

Each of operational amplifiers 19 to 22 has an OFF-signal input terminal, and is rendered to be in an inactive state, where its power consumption becomes zero, by a signal supplied to the OFF-signal input terminal. When the operational amplifiers are rendered to be in the inactive state, their

output terminals become high in impedance.

Each of operational amplifiers 19 to 22 has a voltage follower structure in which its output returns to the inverted side (-) input terminal. When these operational amplifiers are in an active state, the voltage level applied to their non-inverted side (+) input is put out as a low output impedance.

The operational amplifier shown in Fig. 2 as an example of each of operational amplifiers 19 and 20 has differential stage 31 and output stage 32, and its electric current is cut off by transistor 33. Its first stage input portion is formed of N-channel MOSFETs 36 and 37. The operational amplifier shown in Fig. 3 as an example of each of operational amplifiers 21 and 22 also has differential stage 41 and output stage 42, and its electric current is cut off by transistor 43. Its first stage input portion is formed of P-channel MOSFETs 46 and 47.

Bias voltage generator 27 generates N-bias voltage Nb and P-bias voltage Pb. It supplies gate bias voltage Nb to N-channel transistors 34 and 35, both of which contribute to a constant current operation in the inside of the operational amplifier shown in Fig. 2 as an example of each of operational amplifiers 19 and 20. It also supplies gate bias voltage Pb to P-channel transistors 44 and 45, both of which contribute to a constant current operation in the inside of the operational amplifier shown in Fig. 3 as an example of each of operational amplifiers 21 and 22. Fig. 4 shows an exemplary embodiment of bias voltage generator 27.

The processor which is not shown in any of the drawings generates power down signal PD for controlling a display power source. Power down signal PD is supplied to the power source circuit shown in Fig. 1. When power down signal PD is "1", N-channel transistor 23 is cut off, and first to fourth operational amplifiers 19 to 22 are rendered to be in an inactive state by means of OR-gate 25 and NOR-gate 26. When power down signal PD is further supplied to bias voltage generator 27, power consumption in generater 27 will be reduced, so that the power consumed by the liquid crystal driving circuit will be reduced.

Power down signal PD becomes "1" under the condition that a display function is not used in the liquid crystal display device. Power consumption in the display system therefore will be reduced by signal PD.

In voltage dividing circuit 18, the resistance value of each of resistors 11, 12, 16 and 17 is set to be R, and the composite resistance value of resistors 13 to 15 is denoted by r. Intermediate voltage levels supplied to non-inverted side (+) input terminals of operational amplifiers 19 to 22 are denoted by "V2H", "V1H", "V3L" and "V2L". Then intermediate voltage levels may be expressed as follows:

$$V2H = \{(3R + r)/(4R + r)\} \cdot V$$
$$V1H = \{(2R + r)/(4R + r)\} \cdot V$$
$$V3L = \{(2R)/(4R + r)\} \cdot V$$
$$V2L = \{R/(4R + r)\} \cdot V$$

The value of the pre-bias may be expressed as follows:

$$\{R/(4R + r)\} \cdot V$$

In the embodiment, "R = 200 KΩ", and resistors 13 to 15 are respectively set to 400 KΩ, 200 KΩ and 100 KΩ. An ON-resistance of each of analogue switches 241 to 243 for short-circuiting resistors 13 to 15 is set sufficiently smaller than the resistance values of resistors 13 to 15, so that it is possible to consider it "0". Therefore, the composite resistance value r of resistors 13 to 15 may be selected from "0Ω", where signals B0 to B2 are all in a "0" level, to 700KΩ, where signals B0 to B2 are all in a "1" level, and may be fixed to the selected value. Namely, it is possible to select a pre-bias value from V/4 to V/7.5.

Frame signal FR is a signal for making the liquid crystal application voltage into an alternating current, and an alternating signal having a duty ratio of 1/2 is supplied when power down signal PD is "0".

During a period when frame signal FR is "1", first and second operational amplifiers 19 and 20 are rendered to be in an inactive state, whereas third and fourth operational amplifiers 21 and 22 are set to be in an active state. In this condition, P-channel transistor 28 is cut off, and N-channel transistor 29 is turned on. Therefore, output V1 has a "0" level, V2 has voltage level "V2L", and V3 has voltage level "V3L".

In contrast, during a period when frame signal FR is "0", first and second operation amplifiers 19 and 20 are set to an active state, whereas third and fourth operational amplifiers 21 and 22 become an inactive state. P-channel transistor 28 is turned on, and N-channel transistor 29 is cut off. Therefore, terminal V1 puts out voltage level "V1H", V2 puts out level "V2H", and V3 puts out level "V".

The relationship between frame signal FR and terminals V1 to V3 is shown in Fig. 5. In the example shown in Fig.5, resistance value R for resistors 11, 12 and resistors 16, 17 is set to be equal with composite resistance value r of resistors 13 to 15. What is shown in Fig.5 is an example in which intermediate voltage levels are obtained at a 1/5 pre-biased condition.

The structural examples of an operational amplifier in which an inactive state can be set in addition to those examples shown in Fig. 2 and

Fig. 3 are shown in Fig. 6 and Fig. 7. In these figures, the parts corresponding to structural elements of Figs. 2 and 3 are denoted by the same numerals.

The power source device having the above structure makes it possible to obtain a display quality which is equal to that obtained by a liquid crystal driving power source circuit using as its buffers operational amplifiers OP1 to OP4 shown in Fig. 13, and to make its power consumption almost half of power consumption consumed by the circuit shown in Fig. 13. In a voltage dividing circuit shown in Fig. 8, at least four resistors (a group of r1, r4, R1 and R4, or a group of r2, r3, R2 and R3) must be simultaneously changed to change the pre-bias value to be applied to the liquid crystals, so that the amount of circuit elements will increase for performing a pre-bias value control by means of a software. In contrast, in a circuit shown in Fig. 1, the same purpose can be achieved only by changing a composite resistance value of resistors 13 to 15 using instruction signals B0 to B2. Therefore, the pre-bias value can be freely set by means of a software control function.

Claims

1. A power source appratus for driving a liquid crystal display device in which a voltage dividing circuit (18) for voltage-dividing a maximum voltage level "V" and a minimum voltage level "0" to generate a plurality of intermediate voltage levels "V2H", "V1H", "V3L", "V2L" needed for the liquid crystal display device, the voltages having the intermediate voltage levels being put out through a plurality of operational amplifiers (19 - 22) as outputs V1 to V3, characterized in that

   said plurality of operational amplifiers are classified into a first group and a second group, switching signal (FR) for alternating-current-driving said liquid crystal display device sets one of the first and second groups into an active state while the other of the groups into an inactive state, and outputs from the operational amplifiers classified into the group which is set to the active state are supplied to segment electrodes and common electrodes of the liquid crystal display device.

2. An apparatus according to claim 1, characterized in that said voltage dividing circuit is formed of a plurality of resistors (11 - 17) serially coupled with each other, those resistors (13 - 15) that are arranged at a central portion of the plurality of resistors form a set of composite resistors, the plurality of resistors forming the composite resistors are each parallel coupled with a switching circuit, and a value of each of the composite resistors is variably set under control of the switching circuits.

3. An apparatus according to claim 1, characterized in that said voltage dividing circuit is formed of a first resistor (11), a second resistor (12), a third group of resistors (13 - 15), a fourth resistor (16), and a fifth resistor (17), all of which are serially connected with each other between the line for the maximum voltage level "V" and the line for the minimum voltage level "0", voltage outputs having intermediate voltage levels "V2H", "V1H", "V3L", and "V2L" are obtained from connecting points between each of the resistors and the group of resistors, and the voltage outputs are respectively supplied to the operational amplifiers (19 - 22).

4. An apparatus according to claim 3, characterized in that said group of resistors is formed of a plurality of resistors (13 - 15) which are respectively parallel connected with switching circuits (241 - 243), a composite resistance value of the third group of resistors is determined under control of the switching circuits so that a pre-bias value is determined.

5. An apparatus according to claim 1, characterized in that said plurality operational amplifiers are each formed to have a voltage follower structure in which their respective outputs return to their respective input sides.

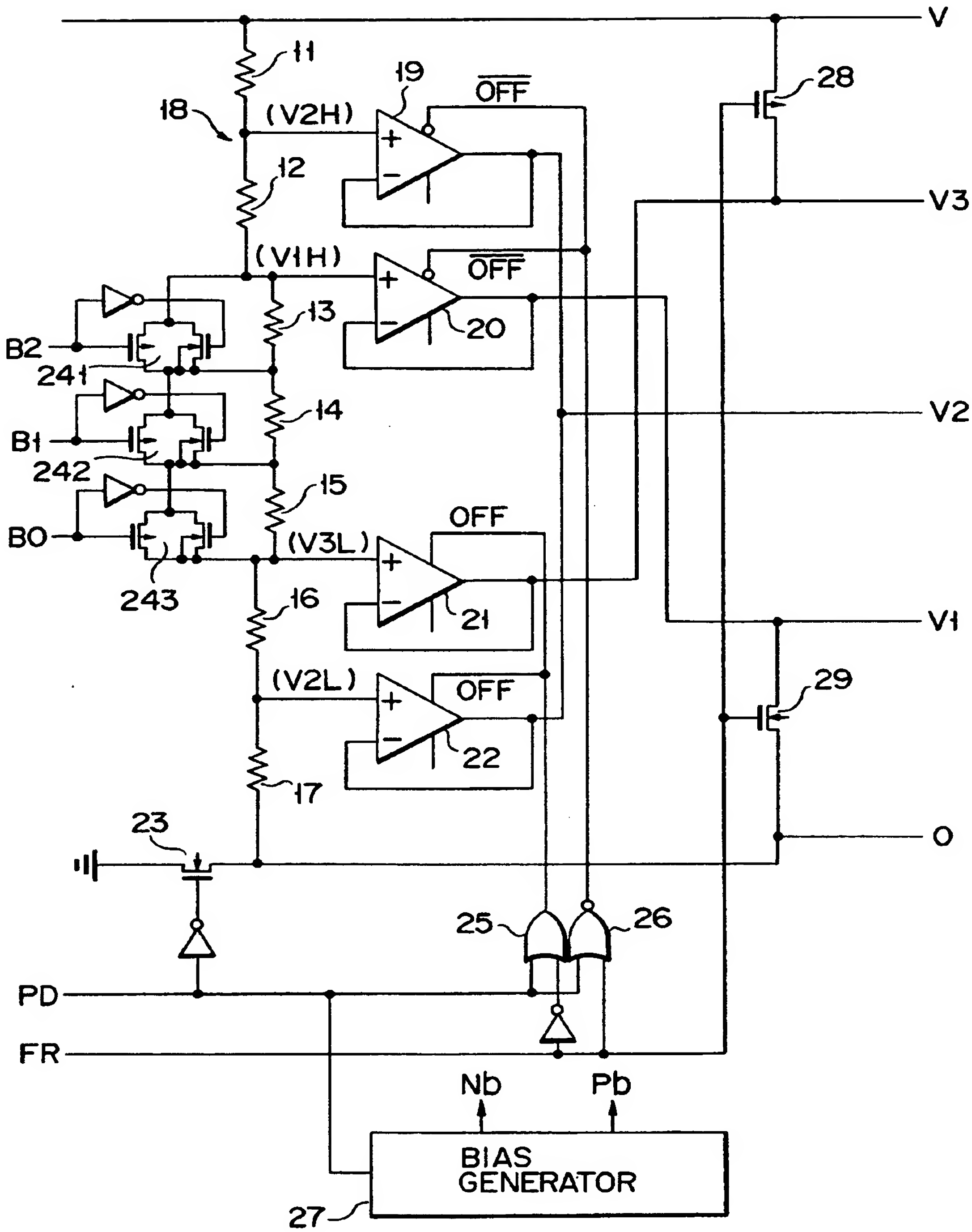
6. An apparatus according to claim 1, characterized in that said plurality of operational amplifiers (19 - 22) are formed such that they are classified into a first group of operational amplifiers (19, 20) and a second group of operational amplifiers (21, 22), first stage input portions of the first group of operational amplifiers are formed of N-channel MOSFETs (36, 37), and first stage input portions of the second group of operational amplifiers are formed of P-channel MOSFETs (46, 47).

7. An apparatus according to claim 1, characterized in that said switching signals are formed of frame signals (FR) which reverse at every display frame unit.

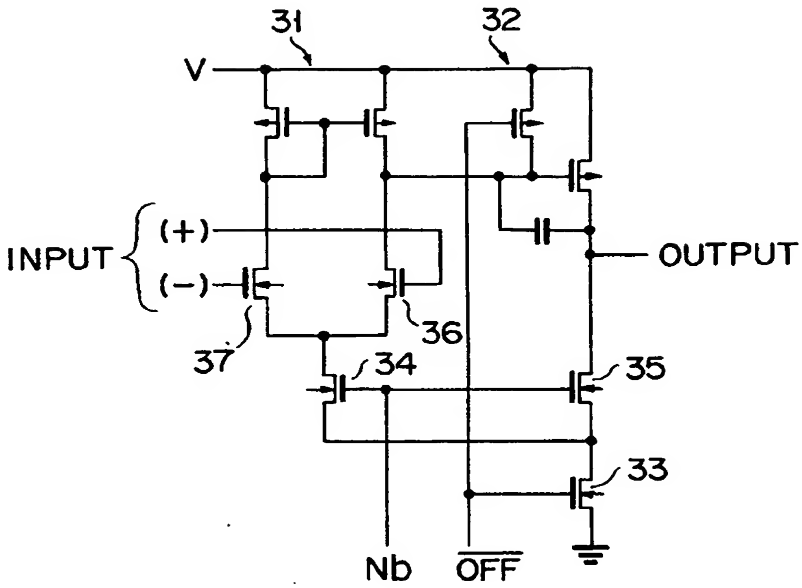
8. An apparatus according to claim 1, characterized in that said operational amplifiers (19 - 22) are set to be in an inactive state while power down signals (PD) for instructing a condition that a display function of the liquid crystal display device is not used are kept sup-

plied.

9. An apparatus according to claim 1, further comprising a bias voltage generator (27) for generating and supplying bias voltage to said operational amplifiers (19 - 22) as bias volatege, the bias voltage generator is set to be in an inactive condition by the power down signal (PD) which is generated under a condition that a display function of the liquid crystal display device is not used.


V
11
19
OFF
18
(V2H)
28
+
-
12
V3
(V1H)
OFF
+
13
-
20
B2
241
14
V2
B1
242
15
OFF
B0
(V3L)
+
243
-
21
16
V1
(V2L)
OFF
29
+
-
22
17
23
O
25
26
PD
FR
Nb
Pb
BIAS
GENERATOR
27

F I G. 1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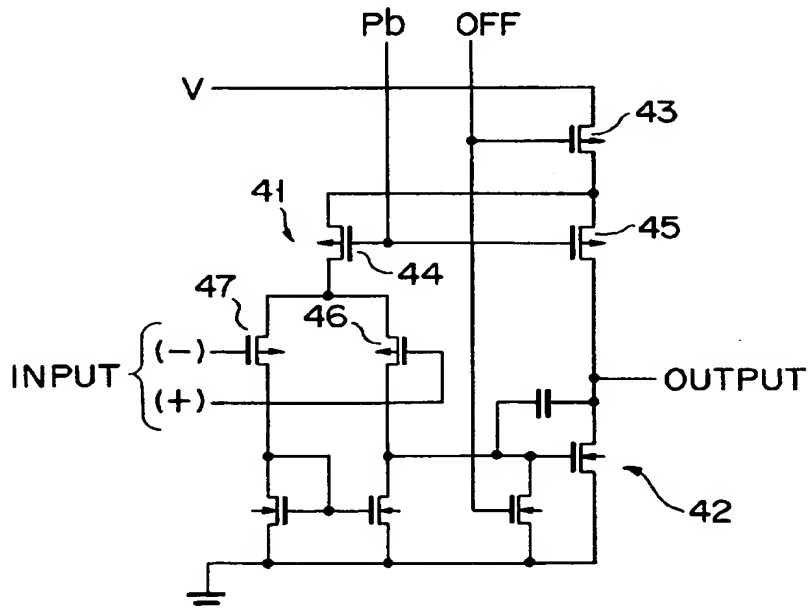
32
V
INPUT
(+)
(−)
OUTPUT
37
36
34
35
33
Nb
OFF

F I G. 2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V
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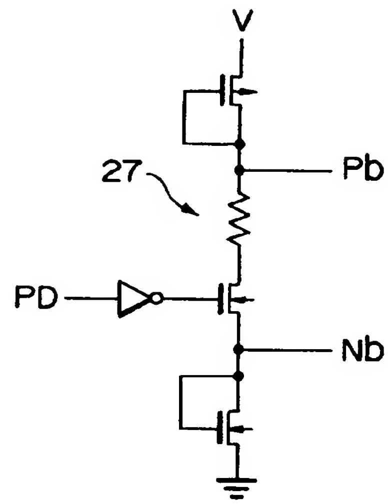
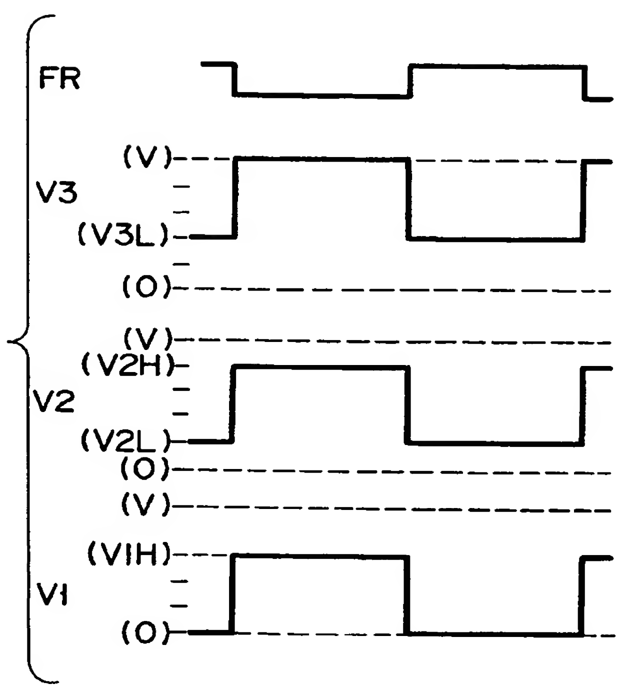
41
45
44
47
46
INPUT
(−)
(+)
OUTPUT
42

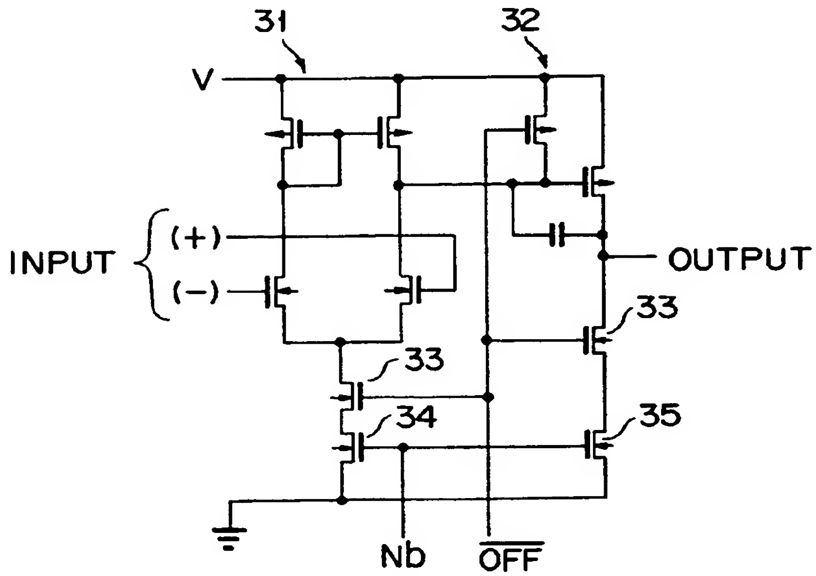
F I G. 3



F I G. 4



F I G. 5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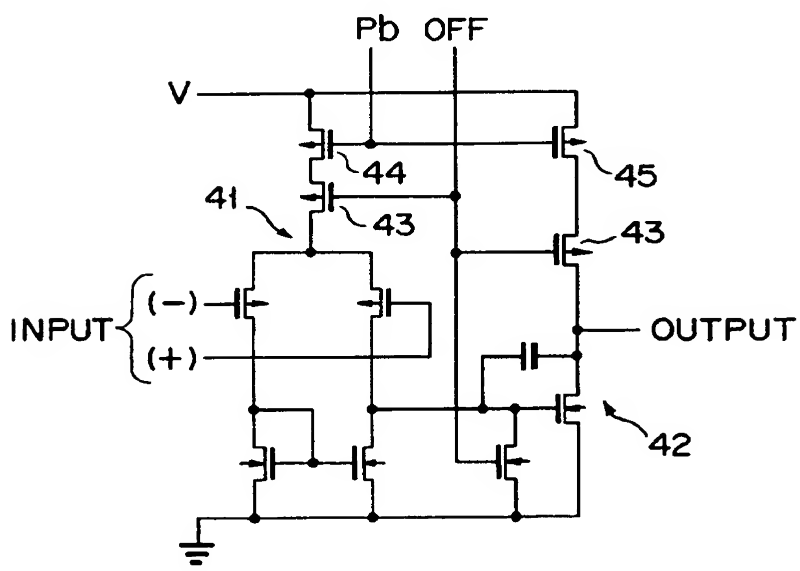
32
V
INPUT
(+)
(−)
OUTPUT
33
33
34
35
Nb
$\overline{OFF}$

F I G. 6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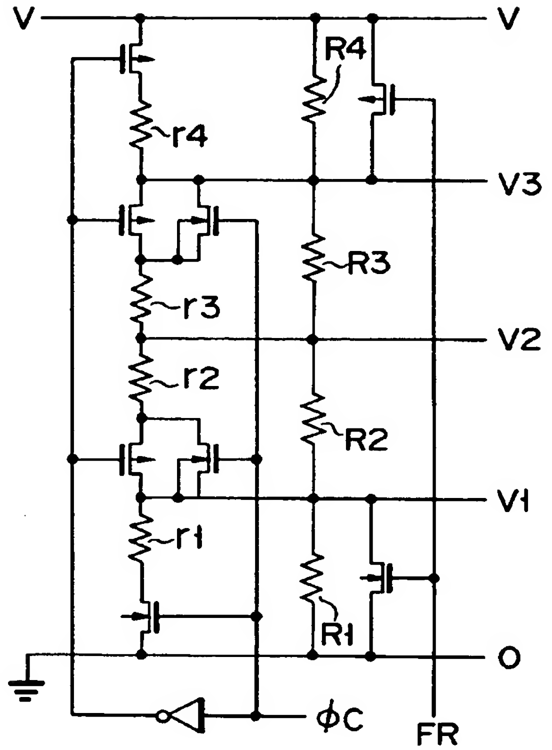
V
44
45
41
43
43
INPUT
(−)
(+)
OUTPUT
42

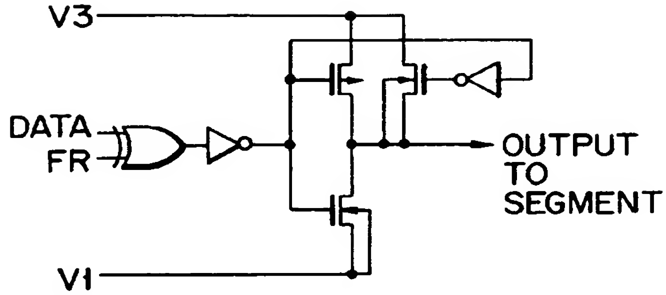
F I G. 7



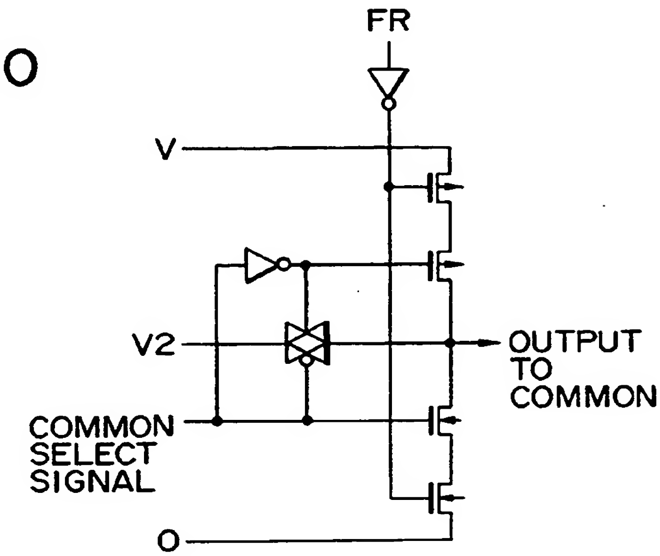
F I G. 8

FR	V1	V2	V3
0	V1H ($=\frac{3}{5}$V)	V2H($=\frac{4}{5}$V)	V
1	0	V2L($=\frac{1}{5}$V)	V3L($=\frac{2}{5}$V)

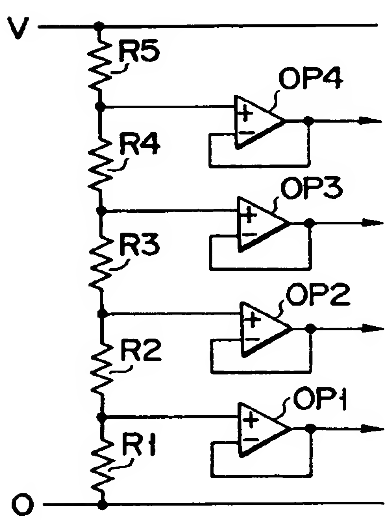
F I G. 9



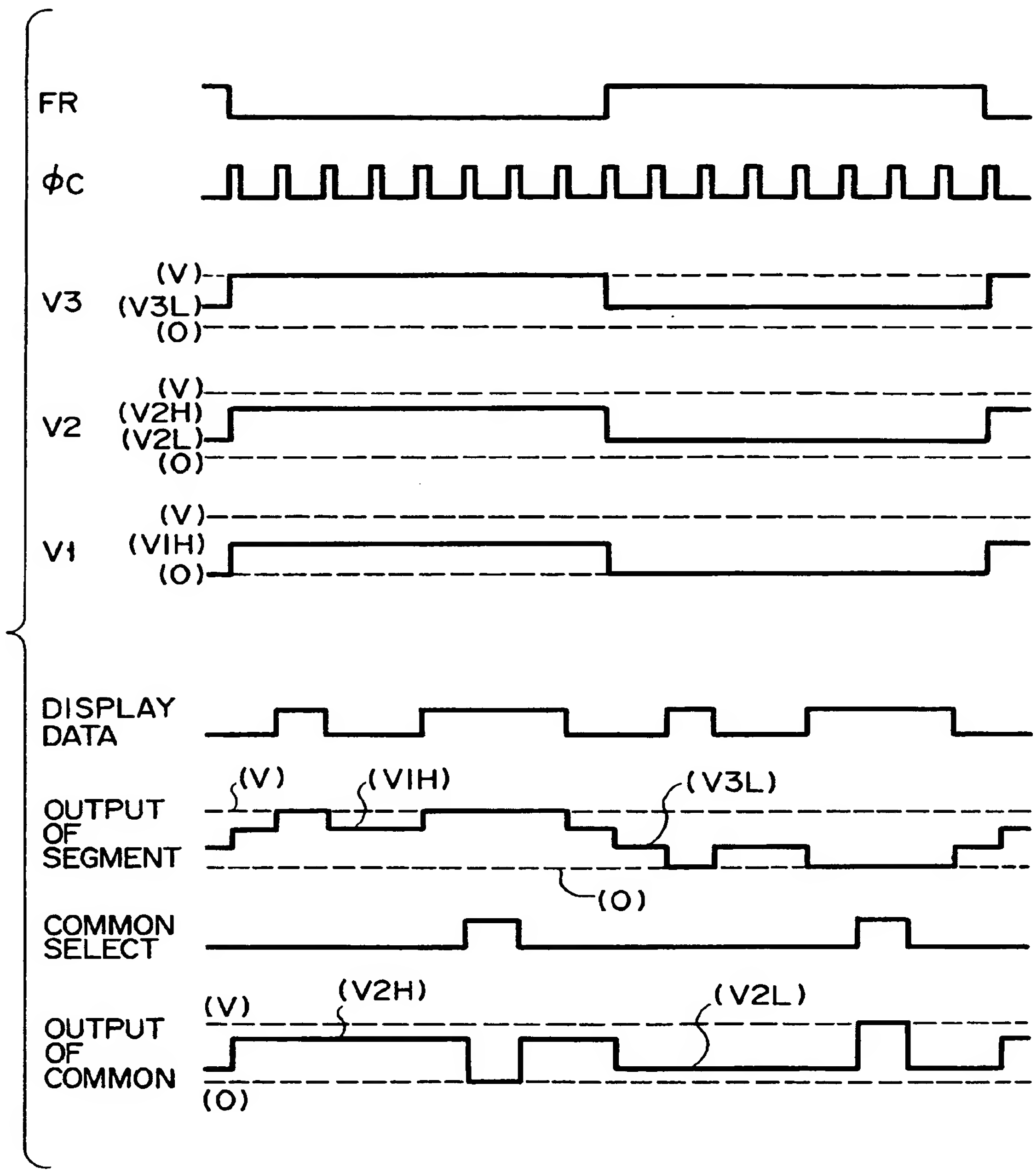
F I G. 10



F I G. 11



F I G. 13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φC
V3
(V)
(V3L)
(O)
V2
(V)
(V2H)
(V2L)
(O)
V1
(V)
(V1H)
(O)
DISPLAY DATA
OUTPUT OF SEGMENT
(V)
(V1H)
(V3L)
(O)
COMMON SELECT
OUTPUT OF COMMON
(V)
(V2H)
(V2L)
(O)

F I G. 12

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Ｇ０２Ｆ　1/133	５２０		Ｇ０２Ｆ　1/133	５２０	

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(54)【発明の名称】　液晶表示器駆動電源回路

(57)【特許請求の範囲】

【請求項１】複数の中間電圧レベルの電極駆動用電圧を発生する液晶表示器駆動電源回路であって、順次、電圧値の異なるV2H、V1H、V3L及びV2Lの中間電圧レベルの電圧を発生する複数の抵抗器を直列接続した電圧分割回路と、前記電圧分割回路から出力される前記V2H、V1H、V3L及びV2Lの中間電圧レベルの電圧がそれぞれ入力され、前記電圧値の順位に対応して２つのグループに分けて設けられる第１乃至第４のオペアンプと、液晶表示器を交流駆動する切り換え信号によって、前記２つのグループに分けて設けられた第１乃至第４のオペアンプを能動状態及び非能動状態に切り換え制御し、表示フレーム毎に反転するフレーム信号に対応して、前記第１及び第２のオペアンプと前記第３及び第４のオペアンプの２つのグループの一方がアクティブ状態とされ他方がノンアクティブ状態とされるように交互に制御するスイッチング信号を発生するオペアンプ制御手段と、前記能動状態に設定される一方のグループの２つのオペアンプからの出力を前記液晶表示器のセグメント電極及びコモン電極に分配結合する駆動電圧出力手段とを具備することを特徴とする液晶表示器駆動電源回路。

【請求項２】前記電圧分割回路は、最高電圧レベル“V”のラインと最低電圧レベル“0”のラインとの間に直列接続された複数の抵抗によって構成され、この複数の抵抗の中央部に配置された抵抗は１組の合成抵抗を構成し、この合成抵抗を構成する複数の抵抗それぞれには並列にスイッチ回路が接続され、このスイッチ回路の制御によって前記合成抵抗値が可変されることを特徴とする請求項１に記載の液晶表示器駆動電源回路。

【請求項３】前記電圧分割回路は、最高電圧レベル“V”

のラインと最低電圧レベル“0″のラインとの間に直列接続された第１乃至第５の抵抗によって構成され、各抵抗の接続点から中間電圧レベル“V2H″、“V1H″、“V3L″及び“V2L″の電圧出力が得られ、各電圧出力が前記第１乃至第４のオペアンプに入力されることを特徴とする請求項１に記載の液晶表示器駆動電源回路。

【請求項４】前記第３の抵抗は、複数の抵抗から構成されると共に、各抵抗に並列にそれぞれスイッチ回路を接続し、このスイッチ回路の制御によって前記第３の抵抗の合成抵抗値が設定され、プリバイアス値が設定されることを特徴とする請求項３に記載の液晶表示器駆動電源回路。

【請求項５】前記第１乃至第４のオペアンプは、第１のグループのオペアンプ及び第２のグループのオペアンプに分けて構成され、前記第１のグループのオペアンプは、初段入力部をＮチャネルMOSFETで構成し、前記第２のグループのオペアンプは、初段入力部をＰチャネルMOSFETで構成するようにしたことを特徴とする請求項１に記載の液晶表示器駆動電源回路。

【請求項６】前記第１乃至第４のオペアンプは、液晶表示器の表示機能を使用しない状態を指示するパワーダウン信号が供給された状態でオフの状態に設定されることを特徴とする請求項１に記載の液晶表示器駆動電源回路。

【請求項７】請求項１に記載の液晶表示器駆動電源回路において、

さらに、バイアス電圧発生回路を備え、前記バイアス電圧発生回路は、バイアス信号を前記第１乃至第４のオペアンプにバイアス信号として供給し、液晶表示器の表示機能を使用しない状態で発生されるパワーダウン信号によって非動作状態に設定されることを特徴とする請求項１に記載の液晶表示器駆動電源回路。

【請求項８】複数の中間電圧レベルの電極駆動用電圧を発生する液晶表示器駆動電源回路であって、第１乃至第５の抵抗を直列接続し、各抵抗の接続点から順次電圧値の異なるV2H、V1H、V3L及びV2Lの中間電圧レベルの電圧が発生されるように前記第１乃至第５の抵抗の直列回路の一端に最高電圧のラインを接続し、前記直列回路の他端に最低電圧のラインを持続することによって構成され、前記第３の抵抗は直列接続した複数の抵抗群によって構成され、前記抵抗群を構成する抵抗はスイッチング回路によって短絡される電圧分割回路と、前記電圧分割回路の第１乃至第５の抵抗の接続点に接続され、前記V2H、V1H、V3L及びV2Lの電圧が入力され、２つのグループに分けられる第１乃至第４のオペアンプと、表示フレーム毎に反転するフレーム信号に対応して、前記第１及び第２のオペアンプを含むグループと前記第３及び第４のオペアンプを含むグループのいずれか一方がアクティブ状態とされ、他方がノンアクティブ状態とされるように交互に制御するスイッチング信号を発生するオペアンプ制御手段と、前記オペアンプ制御手段からの指令に基づいてアクティブ状態とされるグループのオペアンプ群からの出力電圧信号を液晶表示器のセグメント電極及びコモン電極に分配結合する駆動電圧出力手段とを具備することを特徴とする液晶表示器駆動電源回路。

【発明の詳細な説明】

［発明の目的］

（産業上の利用分野）

本発明は液晶表示器の駆動信号を発生させる液晶表示器駆動電源回路に関する。

（従来の技術）

従来、液晶表示器のダイナミック駆動は、最高電位電源と最低電位電源のほか、これらの電位の間の電圧レベル（以下中間電圧レベルと記す）を通常４つ用意し、表示データにしたがって適切な電圧レベルを液晶表示器の各セグメント端子と各コモン端子に印加することにより行なわれる。この中間電圧レベルは、抵抗器による電圧分割によって生成されるのが一般的である。第８図に示す従来回路例では、液晶印加電圧を交流化するためFR信号によって、第９図の図表、第12図の波形からも分かるように、FR＝０の時の最高電位Ｖ、中間電圧レベルV2H, V1H、最低電位０の組と、FR＝１の時の最高電位Ｖ、中間電圧レベルV3L, V2L、最低電位０の組とを交互に発生させ、これらの電圧は第10図のセグメント出力レベル選択回路、第11図のコモン出力レベル選択回路を通じて液相表示器に印加される。この回路例は1/5プリバイアスの場合で、R1＝R4＝300kΩ, R2＝R3＝100kΩ, r1＝r4＝30kΩ, r2＝r3＝10kΩとした。第12図の波形はコモン出力を８本持つ1/8デューティの場合を示している。第12図には複数のセグメント出力とコモン出力のうちのそれぞれ１本のみを例示した。

この回路において、φＣ信号はコモン選択信号の切換タイミングを示すパルス信号であって、コモン信号の切換時に電圧分割回路の出力抵抗を下げて、液晶の応答を早くするためのものである。すなわち、電圧Ｖを分割する抵抗R1, R2, R3, R4に低い抵抗値を持つ抵抗r1, r2, r3, r4を並列に接続することにより、液晶表示器のもつキャパシタンスに対する充放電時間を短縮させようとする。

（発明が解決しようとする課題）

しかしながら、表示画素数の多い液晶表示器は、そのキャパシタンスが大きく、電圧分割回路の出力抵抗を充分に小さくしないと満足な表示品位を得られないが、電圧分割回路の抵抗を小さくすると、消費電流が増大するという欠点がある。

中間電圧レベル電源の出力抵抗を小さくするためにオペアンプを使用した例を第13図に示す。この回路は1/5プリバイアスの場合の例で、R1＝R2＝R3＝R4＝R5である。この第13図の回路ではオペアンプOP1～OP4は常に能動状態であって、消費電流は大きい。

そこで本発明は、充分な表示品位が得られるように出

力抵抗が小さく、かつ消費電力が小さい液晶表示器駆動用の電源を得ることを目的とする。

(課題を解決するための手段と作用)

本発明は、

（１）液晶表示器に必要とされる中間電圧レベルを発生させる電圧分割回路と、該回路の電圧を入力としてボルテージフォロア動作を行なうオペアンプとを有し、該オペアンプは、液晶印加電圧を交流化するための信号に応じて前記オペアンプの出力が液晶電源として使用されない期間には、不使用のオペアンプを機能させる電流が低減化されるものであることを特徴とする液晶表示器駆動電源回路である。また本発明は、

（２）前記中間電圧レベルを発生させる電圧分割回路は、該回路の一部の抵抗を更に細分化してその抵抗を、外部からの信号によるスイッチ動作で選択的に機能させる上記（１）に記載の液晶表示器駆動電源回路である。

即ち本発明は、オペアンプとして、外部からの信号によって消費電力を削減する機能を持ったものを用い、液晶表示器駆動に必要な中間レベル電圧を低い出力抵抗で出力できるようにしておく。液晶印加電圧を交流化するための信号によって、ある中間レベル電圧が電源として不要である期間は、その中間レベル電圧を出力するオペアンプの消費電力を減少させる。これにより、すべてのオペアンプを能動状態にする第13図のような場合よりも、消費電力を小さくできる。また本発明は上記（２）の構成で、所定プリバイアスを得る電圧分割回路の抵抗値を、簡単なソフトウェアで実現できるようにしたものである。

(実施例)

以下図面を参照して本発明の一実施例を説明する。Ｃ－MOS集積回路による液晶表示器駆動回路内蔵ワンチップマイクロコンピュータに適用した本実施例の電源回路を第１図に示す。この電源回路で生成される中間電圧レベルは、V3, V2, V1の各点より出力され、第10図に示したセグメント出力レベル選択回路、第11図に示したコモン出力レベル選択回路に供給されている。オペアンプ１及び２は、初段入力部にＮチャネルMOSFETを使用したオペアンプ、オペアンプ３及び４は、初段入力部にＰチャネルMOSFETを使用したオペアンプであり、その回路の詳細をそれぞれ第２図、第３図に示す。これらのオペアンプは、OFF（オフ）信号入力端子を持ち、この入力信号により、電力消費が０であるオフ状態とすることができる。またオフ状態においては、出力端子が高インピーダンス状態になるという特徴がある。各オペアンプは出力を－入力に帰還させたボルテージフォロワ構成になっており、能動状態であれば＋入力に印加された電圧レベルが低い出力インピーダンスで出力に現われる。

第２図のオペアンプは、差動段21、出力段22とを有し、トランジスタ23でオペアンプ電流をカットオフ可能としている。また第３図のオペアンプは差動段31、出力段32を有し、トランジスタ33でオペアンプ電流をカットオフ可能としている。

バイアス電圧発生回路５は、オペアンプ内部で定電流動作をさせるＮチャネルのトランジスタ24, 25及びＰチャネルのトランジスタ34, 35に対してそれぞれゲートバイアス電圧Nbias及びPbiasを供給している。このための回路の詳細を第４図に示す。オペアンプの入力となる電圧レベルは抵抗8, 9, 10, 11, 12, 13, 14により電源電圧Ｖを分割する電圧分割回路18で得ている。ここで、抵抗10, 11, 12は第13図の抵抗R3に相当し、これら抵抗には、それを短絡するためのアナログスイッチS0, S1, S2があり、抵抗10, 11, 12の合成抵抗値が、CPU部から送られるB2, B1, B0によって決定されるように構成されている。これによって、液晶に印加されるプリバイアス値をプログラムによって設定できる。CPU部からはさらに、表示用電源制御のためのＰDOWN信号が入力される。この信号が“1”レベル（電源電圧Ｖのレベル）の場合には、Ｎチャネルトランジスタ15がカットオフするとともに、ゲート回路16, 17を通じて、４つのオペアンプ１～４をオフ状態とし、さらに、バイアス電圧発生回路５の消費電流をカットすることにより液晶駆動回路の電力消費を完全に抑える。すなわち表示機能を使用しないときには、ＰDOWN信号の“1”とすることでシステムの消費電力を削減できる。抵抗8, 9, 13, 14の抵抗値は等しい、この値をＲとし、抵抗10, 11, 13の合成抵抗値をｒとする。オペアンプ1, 2, 3, 4の＋入力端子に印加される中間電圧レベルをそれぞれV2H, V1H, V3L, V2Lと表わせば、

$$V2H = \frac{3R + r}{4R + r} V$$

$$V1H = \frac{2R + r}{4R + r} V$$

$$V3L = \frac{2R}{4R + r} V$$

$$V2L = \frac{R}{4R + r} V$$

である。またプリバイアスの値は、

$$\frac{R}{4R + r} V$$

である。本実施例ではＲ＝200kΩ、抵抗10, 11, 12をそれぞれ400kΩ, 200kΩ, 100kΩに設定している。抵抗10, 11, 12を短絡しているアナログスイッチS0～S2のオン抵抗はこれらの抵抗値よりじゅうぶん小さく、ほぼ０とみなせるように設計されている。したがって合成抵抗値ｒは（B2, B1, B0）＝（0, 0, 0）の場合の０から（B2, B1, B0）＝（1, 1, 1）の場合の700kΩまで可変できる。すなわち

プリバイアスの値では、V/4からV/7.5まで選択できる。FR信号は、液晶印加電圧を交流化するための信号であり、ＰDOWN信号が“0”の時には、デューティ比が1/2の交番信号が加えられている。FR信号が“1”の帰還では、オペアンプ1,2はオフ状態となり、オペアンプ3,4が能動状態となる。またＰチャネルトランジスタ６はカットオフし、Ｎチャネルトランジスタ７は導通する。したがって、V1点は０レベル（グランドレベル）、V2点はV2Lレベル、V3点はV3Lレベルをそれぞれ出力する。一方、FR信号が“0”の期間では、オペアンプ1,2は能動状態、オペアンプ3,4はオフ状態となり、Ｐチャネルトランジスタ６が導通し、Ｎチャネルトランジスタ７はカットオフする。したがって、V1点はV1Hレベル、V2点はV2Hレベル、V3点はＶレベル（電源電圧レベル）をそれぞれ出力する。以上のことより、FR信号とV1,V2,V3の各点の出力電圧レベルの関係は第５図に示すタイミングチャートに表わすことができる。第５図では、抵抗8,9,13,14の抵抗値Ｒと抵抗10,11,12の合成抵抗値ｒとが等しい、1/5プリバイアスの場合の中間電圧レベルを例として示している。

なお、オフ状態を持たせたオペアンプとしては、第２図、第３図のほかに、第６図、第７図に示すものが考えられる。ここで互に対応する個所には対応符号を用いかつダッシュを付しておく。

上記実施例によれば、第13図の如きオペアンプをバッファとして用いた液晶電源回路で得られるのと同じ表示品位が得られ、しかも、その消費電流はほぼ半減させることができる。また第８図に示す電圧分割抵抗回路では、液晶に加えるプリバイアス値を変化させるためには、少なくとも４つの抵抗値（r1,r4,R1,R4あるいはr2,r3,R2,R3）を同時に変化させる必要があり、ソフトウェアによるプリバイアス値制御を行なうためには回路要素の量がきわめて多くなる欠点があるが、第１図の回路では、CPUからの制御信号B0～B2で実質的に１つの抵抗値（第13図のR3に相当する抵抗10～12）を変化させるだけですみ、容易にソフトウェア制御機能を実現できる特長がある。

［発明の効果］

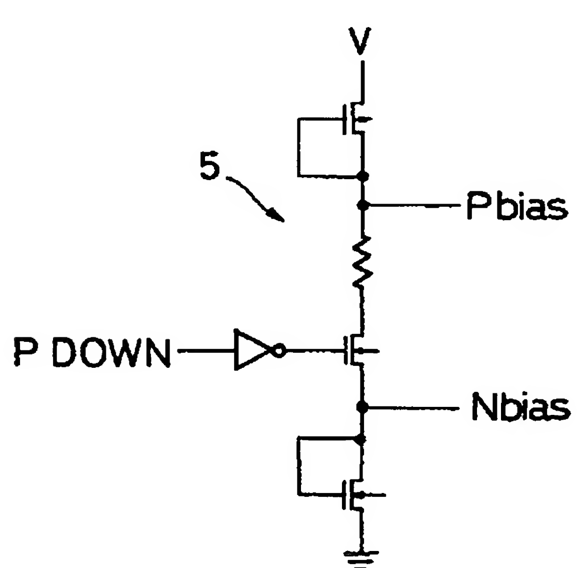
以上説明した如く本発明によれば、充分な表示品位が得られるように出力抵抗が小さく、かつ低消費電力化が可能で、また所定電圧を得る抵抗値制御が簡単な液晶表示器駆動電源回路が提供できる。

【図面の簡単な説明】

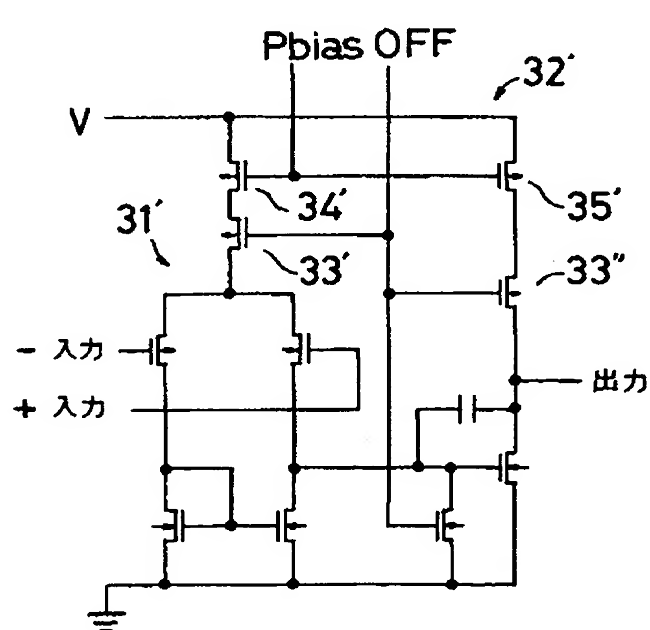
第１図は本発明の一実施例の回路図、第２図ないし第４図は同回路の一部詳細図、第５図は同回路の作用を示す波形図、第６図、第７図は第２図、第３図の変形例の回路図、第８図は従来例の回路図、第９図は同回路の作用を示す図表、第10、第11図は液晶表示に必要な他の回路図、第12図は第８図ないし第11図の各部のタイミング波形図、第13図は第１図を得る前段階の回路図である。

1,2,3,4……消費電流の制御可能なオペアンプ、５……オペアンプ用のバイアス電圧発生回路、６……Ｐチャネルトランジスタ、７……Ｎチャネルトランジスタ、8,9,10,11,12,13,14……中間電圧レベルを発生させる電圧分割用抵抗、15……表示回路電源スイッチ用トランジスタ、16,17……オペアンプの消費電流制御信号を生成するゲート回路、18……電圧分割回路、23,33……オペアンプ電流カット用トランジスタ、S0～S2……アナログスイッチ。

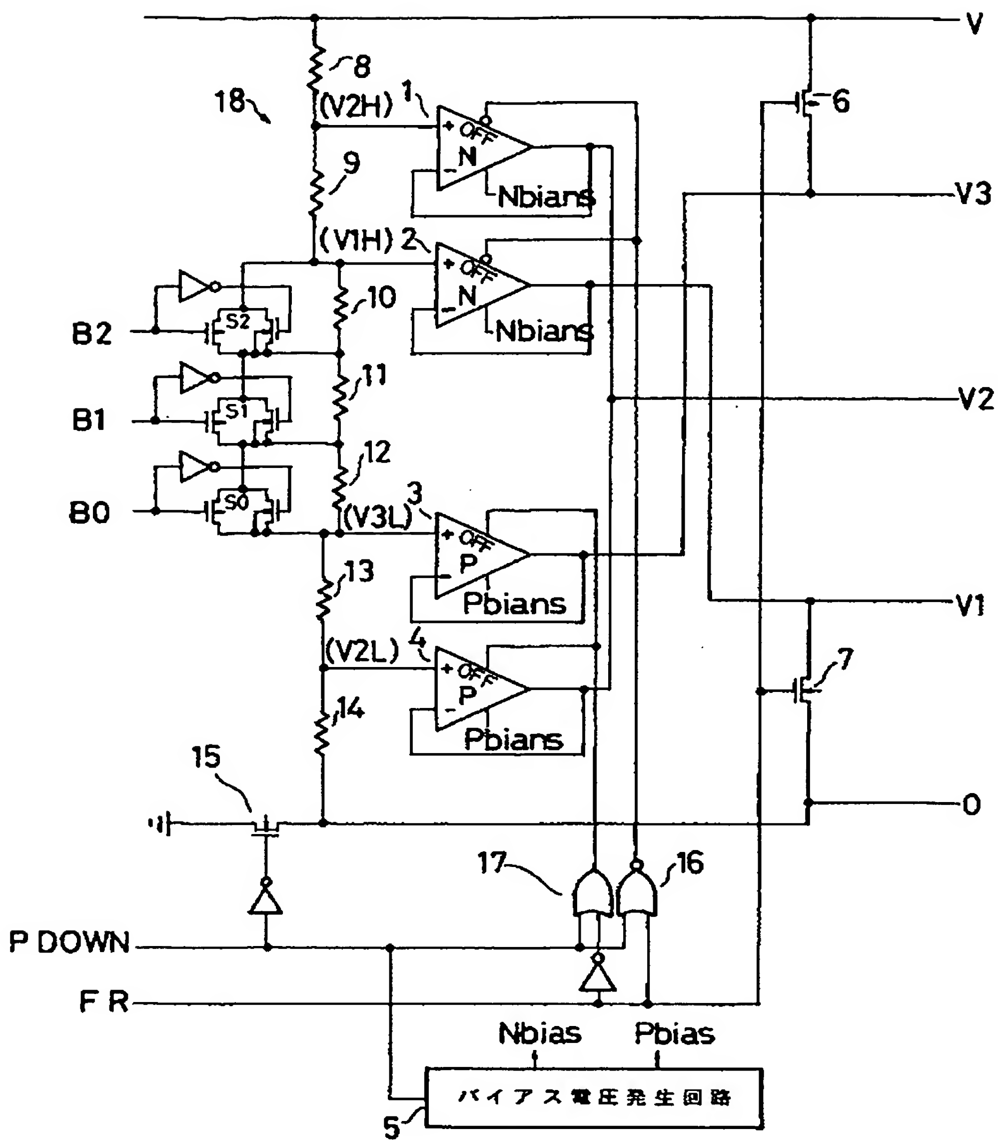
【第４図】



【第７図】



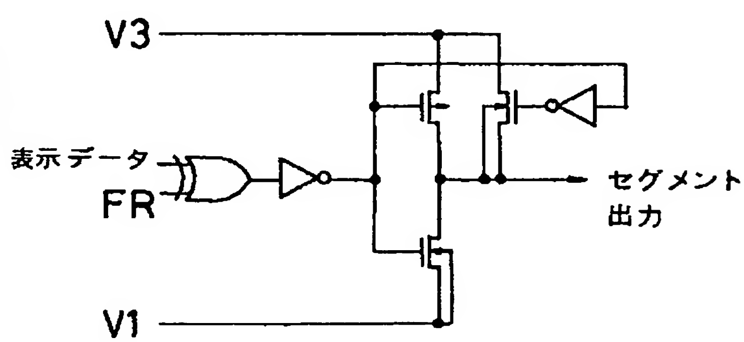
【第１図】



【第９図】

FR	V1	V 2	V3
"0"	VIH(=3/5v)	V2H(=4/5v)	V
"1"	V	V2L(=1/5v)	V3L(=2/5v)

【第１０図】



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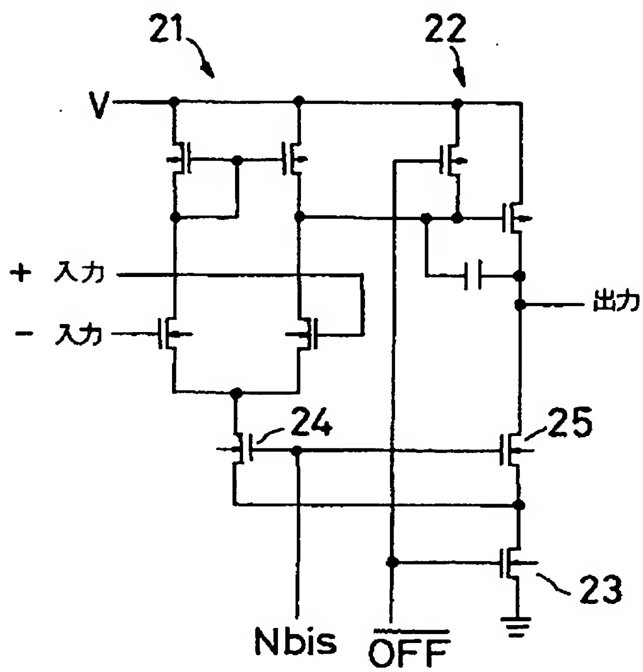

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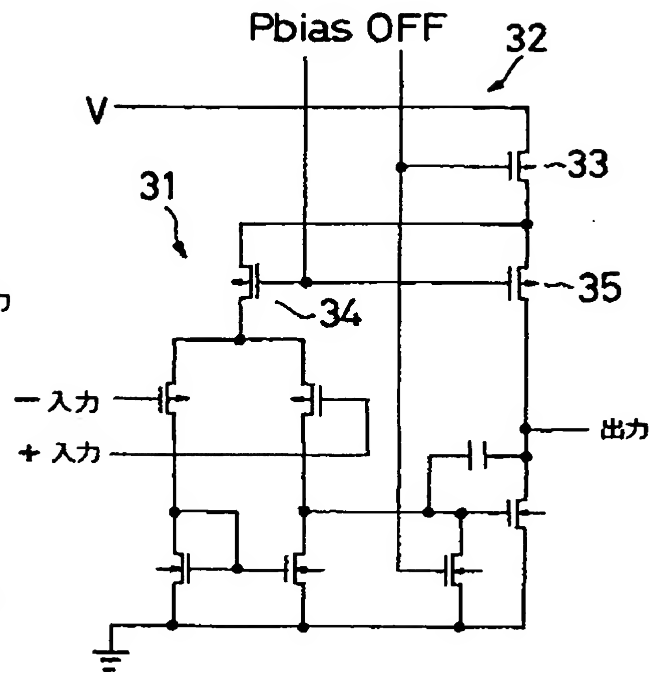
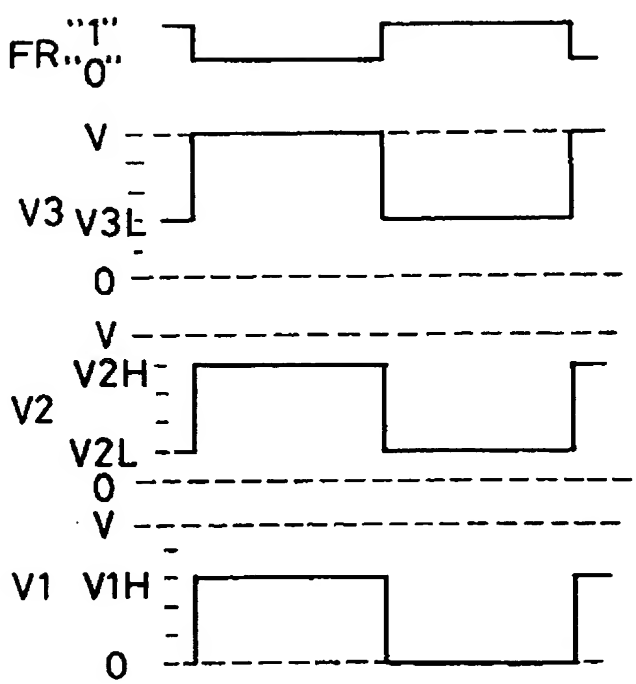


【第５図】



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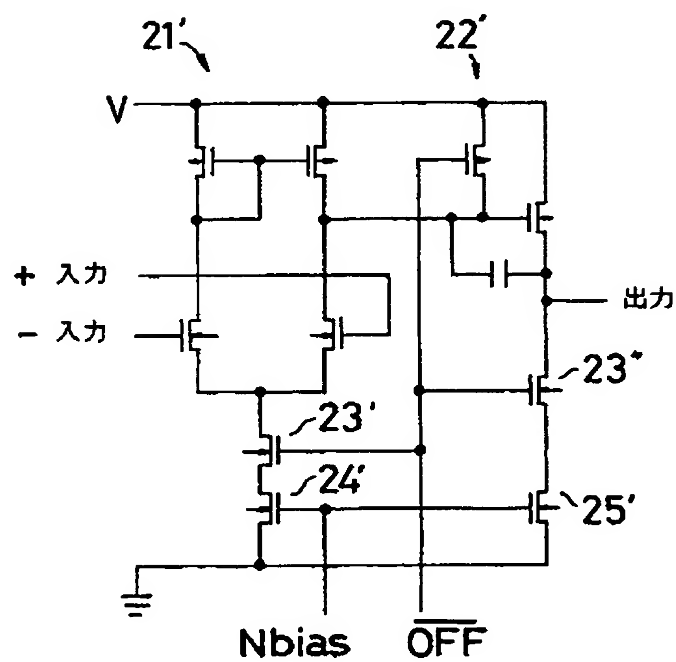
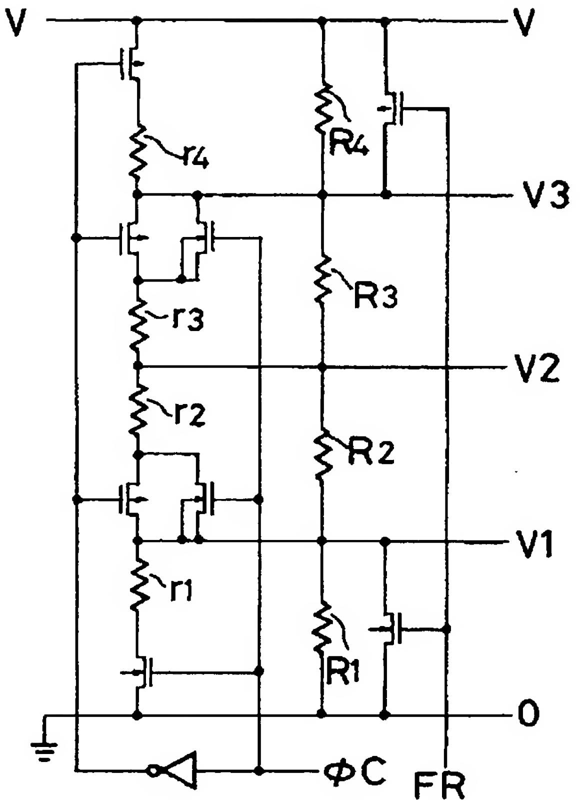
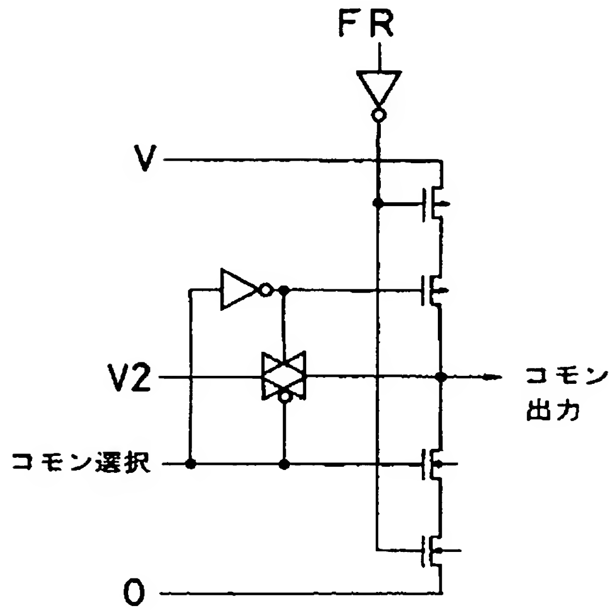


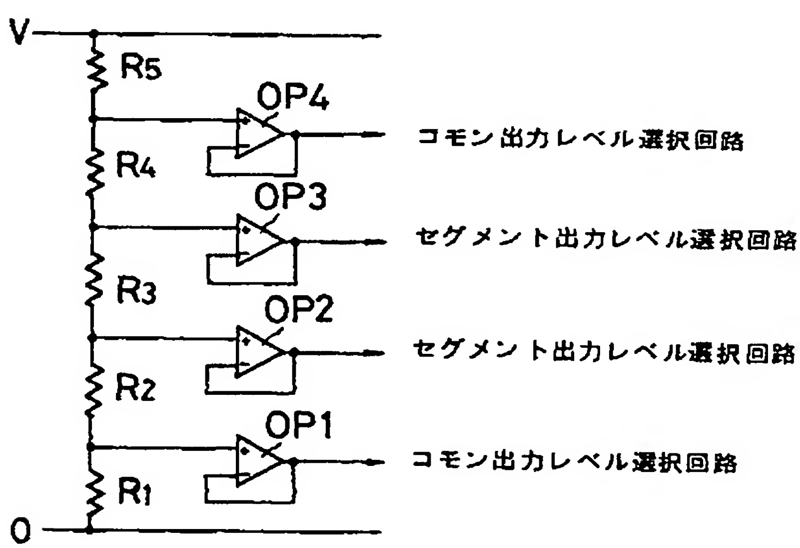
【第８図】



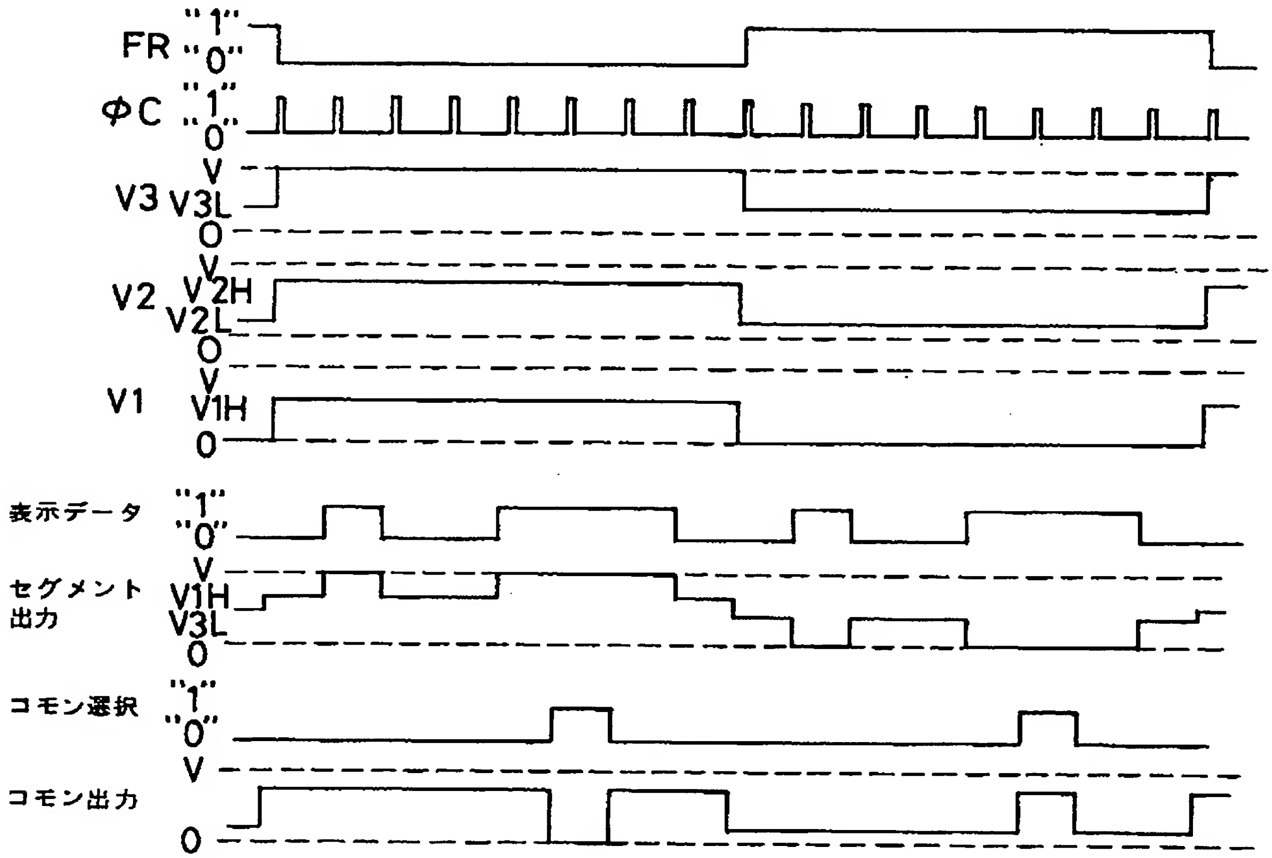
【第１１図】



【第１３図】



【第１２図】


FR
"1"
"0"
ΦC
"1"
"0"
V
V3
V3L
0
V
V2
V2H
V2L
0
V
V1
V1H
0
表示データ
"1"
"0"
V
セグメント出力
V1H
V3L
0
コモン選択
"1"
"0"
V
コモン出力
0